Abstracts

A Heterostructure FET with 75.8-Percent Power Added Efficiency at 10 GHz

P. Saunier, W.S. Kopp, H.Q. Tserng, Y.C. Kao and D.D. Heston. "A Heterostructure FET with 75.8-Percent Power Added Efficiency at 10 GHz." 1992 MTT-S International Microwave Symposium Digest 92.2 (1992 Vol. II [MWSYM]): 635-638.

We are reporting the performance of a new AIGaAs/GaAs heterostructure FET (HFET), designed to have very high efficiency at X-band with high drain bias (9 volts and above). The combination of low doped (high 10/sup 16/ cm/sup -3/)AlGaAs under the gate and highly doped (mid 10/sup 17/ cm/sup -3/) GaAs channel and superlattice buffer layer allow high gate-drain and source-drain breakdown voltage (more than 20 volts), constant transconductance and moderate to high maximum channel current (350 to 450 mA/mm). These characteristics make the devices ideal for Class B and Class F operation. The 1200 x 0.25-µm HFET devices have demonstrated a record power-added efficiency (PAE) of 75.8 percent with 603 mW of outputpower and 8.8 dB of gain with a 9-volt drain bias at 10 GHz. Other 1200 x 0.25-µm HFET devices have demonstrated 63.2-percent PAE with 8.3 dB of gain and 851 mW of output power with a 12-volt drain bias. At 14 volts, we have measured 50-percent PAE with 7.4-dB gain and 1.1 watts of output power.

❑ Return to main document.